IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A semiconductor memory device comprising:

word lines formed along a first direction;

bit lines formed along a second direction which intersects the first direction;

memory cells including magneto-resistive elements and arranged at intersections of the word lines and the bit lines;

a row decoder which selects at least one of the word lines;

a column decoder which selects at least one of the bit lines; and

a write circuit which supplies first and second write currents to a selected word line and selected bit line selected by the row decoder and column decoder respectively and writes data into a selected memory cell arranged at the intersection of the selected word line and the selected bit line, the write circuit ~~changing the current values of the first and second write currents according to a temperature change~~ including first and second current sources whose supply currents have different temperature dependencies, the first and second current sources being set to be one of an enable state and a disable state in accordance with an ambient temperature, at least one of current values of the first and second write currents being controlled in accordance with the supply currents of the first and second current sources.

Claims 2-6 (Canceled).

Claim 7 (Original): The device according to claim 1, further comprising a write current setting circuit which searches for optimum current values of the first and second write currents according to a temperature;

a holding circuit which holds information relating to the current values of the first and second write currents obtained by the write current setting circuit together with temperature data; and

a readout circuit which reads out information held in the holding circuit according to a temperature,

wherein the write circuit supplies the first and second write currents based on the information read out from the holding circuit by the readout circuit.

Claim 8 (Original): The device according to claim 7, further comprising a data pattern generator which generates a data pattern to be written into the memory cell when optimum current values of the first and second write currents are searched for according to the temperature,

wherein the current setting circuit includes: a comparator circuit which compares the data pattern generated from the data pattern generator with readout data read out from the memory cell; and

a count circuit which counts the number of times which the result of comparison by the comparator circuit has indicated coincidence, and

the holding circuit holds information relating to current values of the first and second write currents obtained when the count number in the count circuit becomes maximum.

Claim 9 (Original): The device according to claim 1, wherein the current values of the first and second write currents are different from each other.

Claim 10 (Original): The device according to claim 1, wherein the write circuit changes a ratio of the current values of the first and second write currents according to a temperature.

Claim 11 (Currently Amended): A semiconductor memory device comprising:

word lines formed along a first direction;

bit lines formed along a second direction which intersects the first direction;

memory cells including magneto-resistive elements and arranged at intersections of the word lines and the bit lines;

a row decoder which selects at least one of the word lines;

a column decoder which selects at least one of the bit lines; and

a write circuit which respectively supplies first and second write currents to a selected word line and selected bit line selected by the row decoder and column decoder and writes data into a selected memory cell arranged at the intersection of the selected word line and the selected bit line; the write circuit ~~changing the current values of the first and second write currents according to a temperature change and changing one of the first and second write currents according to write data~~ including a plurality of first MOS transistors which generate the first write current and a plurality of second MOS transistors which generate the second write current, the number of transistors to be set in an ON state being changed in accordance with an ambient temperature at least in one of the first and second MOS transistors.

Claim 12 (Currently Amended): The device according to claim 11, wherein the write circuit ~~includes first and second MOS transistors which respectively supply the first and second write currents to the selected word line and selected bit line; and~~

~~a current source circuit which supplies currents to the first and second MOS transistors by current mirror; and~~

~~the supply currents have a temperature dependency~~ includes first and second current sources whose supply currents have different temperature dependencies, the first and second current sources are set to be one of an enable state and a disable state in accordance with an ambient temperature, and at least one of current values of the first and second write currents is controlled in accordance with the supply currents of the first and second current sources.

Claim 13 (Canceled).

Claim 14 (Currently Amended): The device according to claim [[13]] 11, further comprising a holding circuit which holds information of MOS transistors to be set in the ON state in the first and second MOS ~~transistor groups~~ transistors for respective temperatures; and

a readout circuit which reads out information from the holding circuit according to a temperature to control ON/OFF states of the MOS transistors in the first and second MOS ~~transistor groups~~ transistors.

Claims 15-20 (Canceled).

Claim 21 (Currently Amended): The device according to claim 11, wherein the write circuit ~~includes a first MOS transistor group which supplies the first write current to the selected word line;~~

~~a second MOS transistor group which supplies the second write current to the selected bit line from one end thereof; and~~

~~a third MOS transistor group which supplies the second write current to the selected bit line from the other end thereof, and~~ further includes a plurality of third MOS transistors which supply the second write current from one end of the selected bit line,

the second MOS transistors supply the second write current from the other end of the selected bit line, and

the number of MOS transistors which are set in an ON state in the first to third MOS transistors decreases with a temperature rise.

Claim 22 (Currently Amended): The device according to claim 21, further comprising a holding circuit which holds information of MOS transistors to be set in the ON state in the first to third MOS ~~transistor groups~~ transistors for respective temperatures; and

a readout circuit which reads out information from the holding circuit according to a temperature to control ON/OFF states of the MOS transistors in the first to third MOS ~~transistor groups~~ transistors.

Claim 23 (Original): The device according to claim 21, further comprising a write current setting circuit which searches for optimum current values of the first and second write currents according to a temperature; and

a holding circuit which holds information relating to the current values of the first and second write currents obtained by the write current setting circuit together with temperature data, and a readout circuit which reads out information held in the holding circuit according to a temperature,

wherein the write circuit supplies the first and second write currents based on the information read out from the holding circuit by the readout circuit.

Claim 24 (Original): The device according to claim 23, further comprising a data pattern generator which generates a data pattern to be written into the memory cell when optimum current values of the first and second write currents are searched for according to the temperature,

wherein the current setting circuit includes a comparator circuit which compares the data pattern generated from the data pattern generator with readout data read out from the memory cell and

a count circuit which counts the number of times which the result of comparison by the comparator circuit has indicated coincidence, and

the holding circuit holds information relating to current values of the first and second write currents obtained when the count number in the count circuit becomes maximum.

Claim 25 (Original): The device according to claim 11, wherein the current values of the first and second write currents are different from each other.

Claim 26 (Original): The device according to claim 11, wherein the write circuit changes a ratio of the current values of the first and second write currents according to a temperature.

Claim 27 (Original): A control method of a semiconductor memory device comprising:

holding data relating to optimum values of first and second write currents respectively supplied to one of a plurality of word lines formed along a first direction and one of a plurality of bit lines formed along a second direction which intersects the first direction to write data into one of memory cells which includes magneto-resistive elements and are

respectively arranged at intersections of the word lines and the bit lines in a holding section according to temperatures;

detecting a temperature at a write time;

reading out data corresponding to the detected temperature from the holding section; and

writing data into the memory cell by causing a word line current source and bit line current source to respectively supply first and second write currents of optimum values to the word line and bit line according to the data read out from the holding section.

Claim 28 (Original): The method according to claim 27, wherein the holding the data relating to the optimum values of the first and second write currents in the holding section according to temperatures includes:

writing a data pattern generated from a data pattern generator into a memory cell array by use of a plurality of the first and second write currents;

verifying data written into the memory cell and holding current values of the first and second write currents obtained when the number of memory cells into which data is correctly written becomes maximum in a first register together with temperature data; and

changing a temperature and returning a process to the writing the data pattern into the memory cell array.

Claim 29 (Original): The method according to claim 28, further comprising initializing values of the first register and a second register before writing the data pattern into the memory cell array,

wherein the word line current source and bit line current source generate the first and second write currents based on the value held in the first register in the writing the data pattern into the memory cell array and

the verifying data written in the memory cell and holding the current values in the first register includes:

reading out data from a memory cell included in the memory cell array;

comparing data read out from the memory cell with the data pattern;

causing a counter to count up a count number thereof when data read out from the memory cell coincides with the data pattern;

comparing the count number of the counter with the value held in the second register after the comparing data and causing the counter to count up for a preset number of memory cells included in the memory cell array are terminated;

rewriting the value of the second register into the count number of the counter and rewriting the value of the first register to a value corresponding to the current values of the first and second write currents used for the writing of the data pattern when the count number of the counter is larger than the value held in the second register; and

changing the current values of the first and second write currents and returning a process to the writing the data pattern.

Claim 30 (Currently Amended): A memory card comprising at least one semiconductor memory cell block,

the semiconductor memory cell block including:

word lines formed along a first direction;

bit lines formed along a second direction which intersects the first direction;

memory cells including magneto-resistive elements and arranged at intersections of the word lines and the bit lines;

a row decoder which selects at least one of the word lines;

a column decoder which selects at least one of the bit lines; and

a write circuit which supplies first and second write currents to a selected word line and selected bit line selected by the row decoder and column decoder respectively and writes data into a selected memory cell arranged at the intersection of the selected word line and the selected bit line, the write circuit ~~changing the current values of the first and second write currents according to a temperature change~~ including first and second current sources whose supply currents have different temperature dependencies, the first and second current sources being set to be one of an enable state and a disable state in accordance with an ambient temperature, at least one of current values of the first and second write currents being controlled in accordance with supply currents of the first and second current sources.

Claim 31 (Original): The card according to claim 30, further comprising a write current setting circuit which searches for optimum current values of the first and second write currents according to a temperature;

a holding circuit which holds information relating to the current values of the first and second write currents obtained by the write current setting circuit together with temperature data;

a readout circuit which reads out information held in the holding circuit according to a temperature; and

a data pattern generator which generates a data pattern to be written into the memory cell when optimum current values of the first and second write currents are searched for according to the temperature,

wherein the write circuit supplies the first and second write currents based on the information read out from the holding circuit by the readout circuit,

the current setting circuit includes a comparator circuit which compares the data pattern generated from the data pattern generator with readout data read out from the memory cell; and

a count circuit which counts the number of times which the result of comparison by the comparator circuit has indicated coincidence, and

the holding circuit holds information relating to current values of the first and second write currents obtained when the count number in the count circuit becomes maximum.

Claim 32 (Currently Amended): A memory card comprising at least one semiconductor memory cell block,

the semiconductor memory cell block including:

word lines formed along a first direction;

bit lines formed along a second direction which intersects the first direction;

memory cells including magneto-resistive elements and arranged at intersections of the word lines and the bit lines;

a row decoder which selects at least one of the word lines;

a column decoder which selects at least one of the bit lines; and

a write circuit which respectively supplies first and second write currents to a selected word line and selected bit line selected by the row decoder and column decoder and writes data into a selected memory cell arranged at the intersection of the selected word line and the selected bit line; the write circuit ~~changing the current values of the first and second write currents according to a temperature change and changing one of the first and second write currents according to write data~~ including a plurality of first MOS transistors which generate

the first write current and a plurality of second MOS transistors which generate the second write current, the number of transistors to be set in an ON state being changed in accordance with an ambient temperature at least in one of the first and second MOS transistors.

Claim 33 (Original): The card according to claim 32, further comprising a write current setting circuit which searches for optimum current values of the first and second write currents according to a temperature;

a holding circuit which holds information relating to the current values of the first and second write currents obtained in the current setting circuit together with temperature data;

a readout circuit which reads out the information held in the holding circuit according to a temperature; and

a data pattern generator which generates a data pattern to be written into the memory cell when optimum current values of the first and second write currents are searched for according to the temperature;

wherein the write circuit supplies the first and second write currents based on the information read out from the holding circuit by the readout circuit,

the current setting circuit includes a comparator circuit which compares the data pattern generated from the data pattern generator with readout data read out from the memory cell; and

a count circuit which counts the number of times which the result of comparison by the comparator circuit has indicated coincidence, and

the holding circuit holds information relating to current values of the first and second write currents obtained when the count number in the count circuit becomes maximum.